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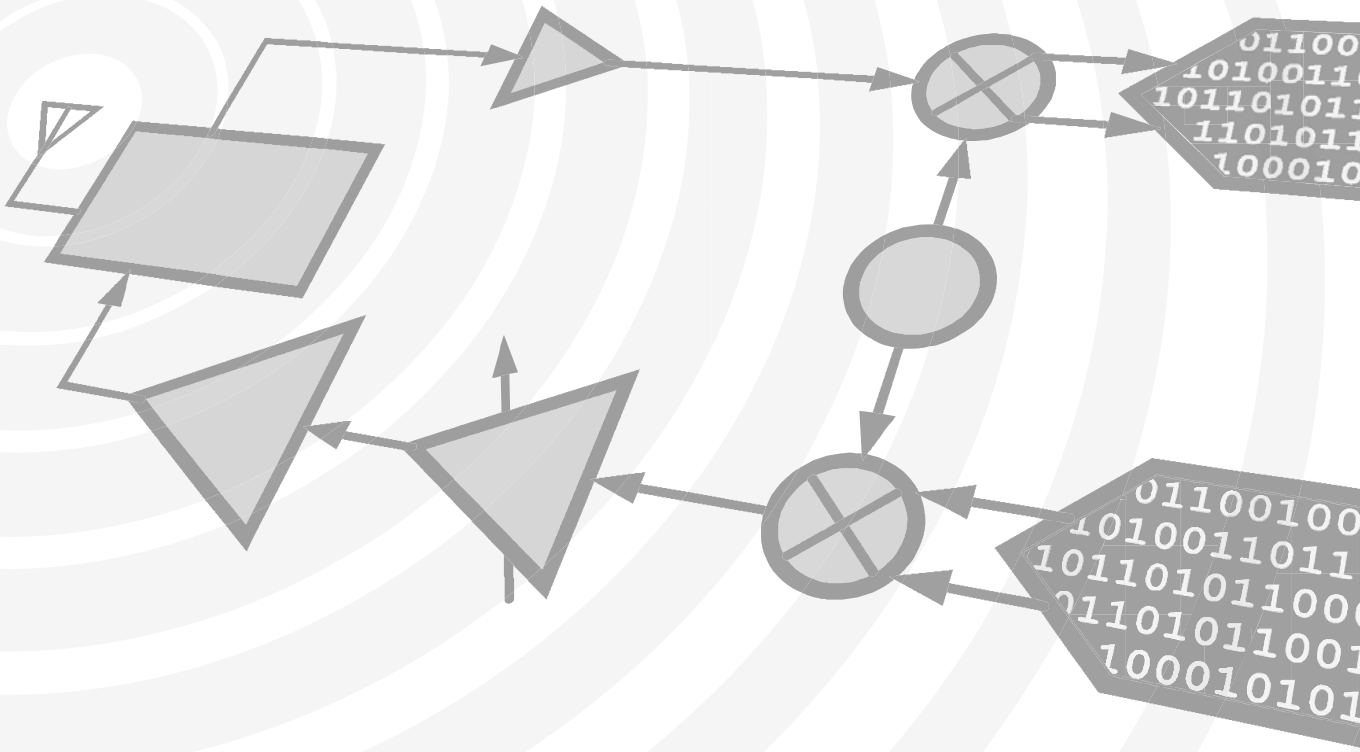

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HMC998LP5E

v01.0813

GaAs pHEMT MMIC 2 WATT POWER AMPLIFIER, 0.1 - 20 GHz

Typical Applications

The HMC998LP5E is ideal for:

- Test Instumentation
- Microwave Radio & VSAT
- Military & Space
- Telecom Infrastructure
- Fiber Optics

Features

P1dB Output Power: +31 dBm

Psat Output Power: +33 dBm

High Gain: 11 dB

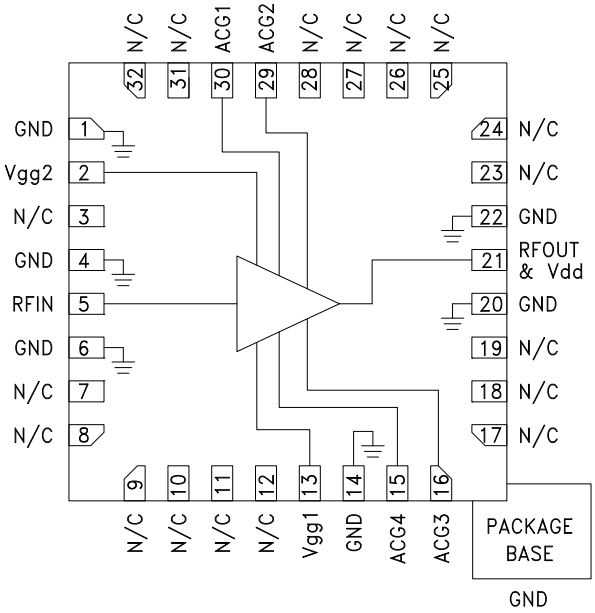
Output IP3: +41 dBm

Supply Voltage: Vdd = +15V @ 500 mA

50 Ohm Matched Input/Output

32 Lead 5x5 mm SMT Package: 25 mm²

Functional Diagram



General Description

The HMC998LP5E is a GaAs pHEMT MMIC Distributed Power Amplifier which operates between 0.1 and 20 GHz. The amplifier provides 11 dB of gain, +41 dBm output IP3, and +31 dBm of output power at 1 dB gain compression while requiring only 500 mA from a +15V supply. The HMC998LP5E exihibits a slightly positive gain from 3 to 17 GHz making it ideal for EW, ECM, Radar and test equipment applications. The HMC998LP5E amplifier I/Os are internally matched to 50 Ohms and is supplied in a leadless QFN 5x5 mm surface mount package.

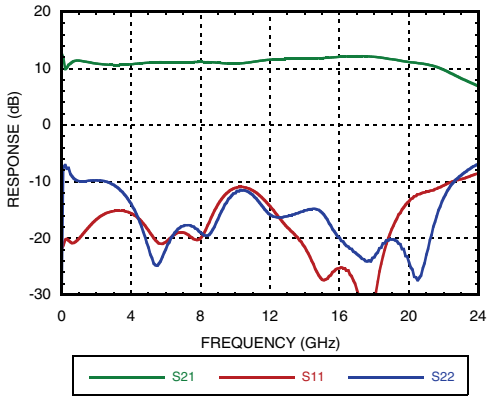
Electrical Specifications, T_A = +25° C, Vdd =+15V, Vgg2 = +9.5V, Idd = 500 mA [1]

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	max	Units
Frequency Range		0.1 - 4			4 - 16			16 - 20		GHz
Gain	8	11		8	11		9	12		dB
Gain Flatness		±0.3			±0.5			±0.5		dB
Gain Variation Over Temperature		0.006			0.012			0.017		dB/ °C
Input Return Loss		17			15			25		dB
Output Return Loss		10			15			20		dB
Output Power for 1 dB Compression (P1dB)	28	31		28	31		26	29		dBm
Saturated Output Power (Psat)		33			33			31		dBm
Output Third Order Intercept (IP3) [2]		41			41			40		dBm
Noise Figure		8			4.5			5		dB
Total Supply Current		500			500			500		mA

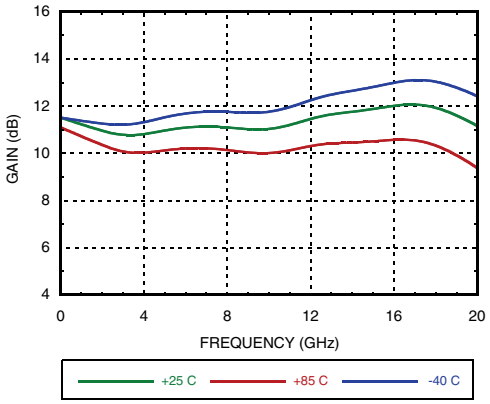
[1] Adjust Vgg between -2 to 0V to achieve Idd = 500 mA typical.

[2] Measurement taken at Pout / tone = +14 dBm.

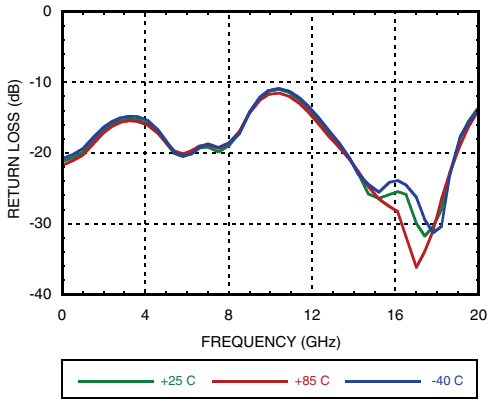
Gain & Return Loss



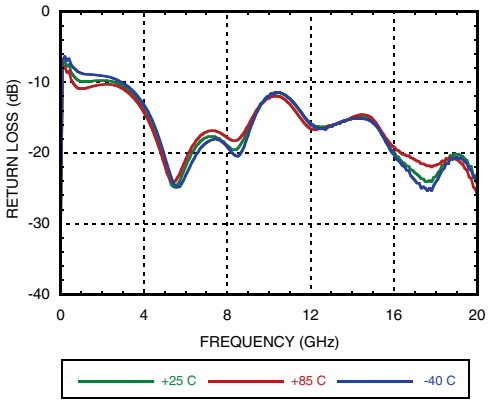
Gain vs. Temperature



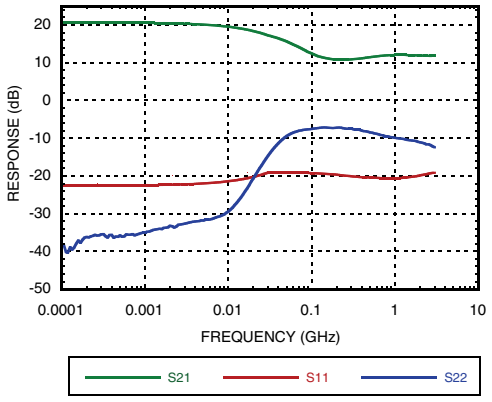
Input Return Loss vs. Temperature



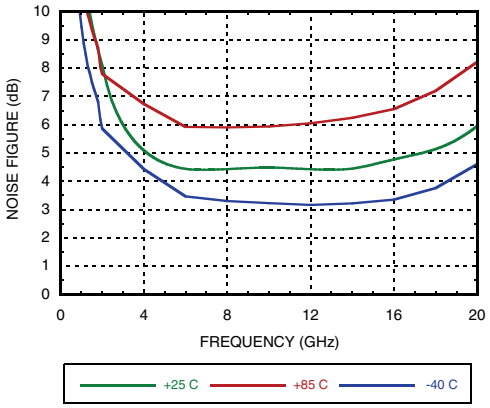
Output Return Loss vs. Temperature



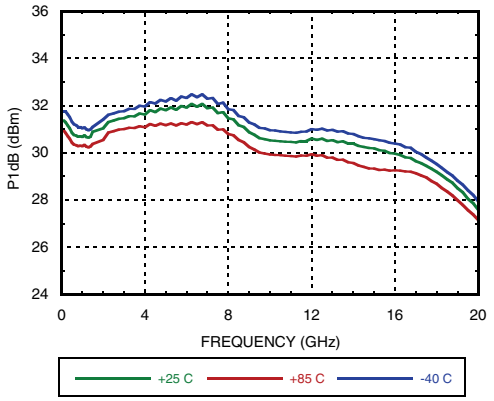
Low Frequency Gain & Return Loss



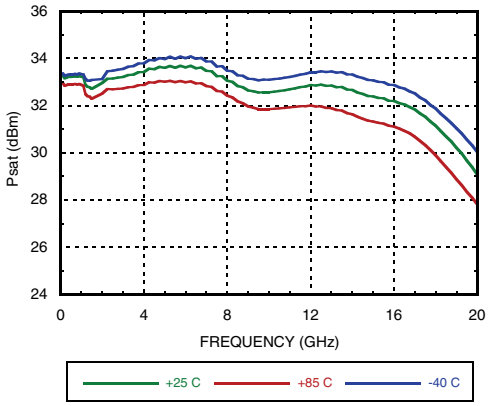
Noise Figure vs. Temperature



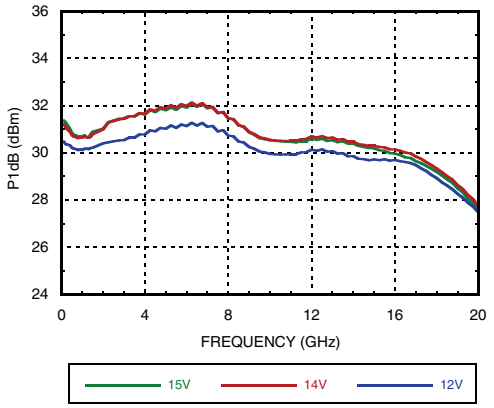
P1dB vs. Temperature



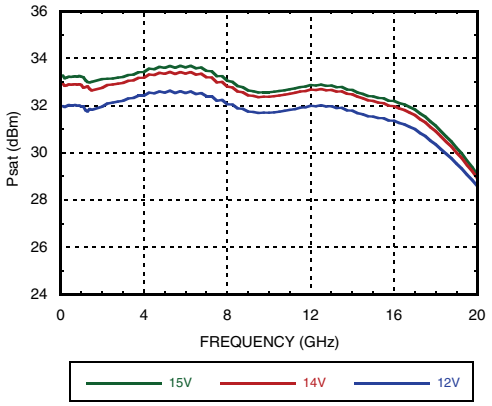
Psat vs. Temperature



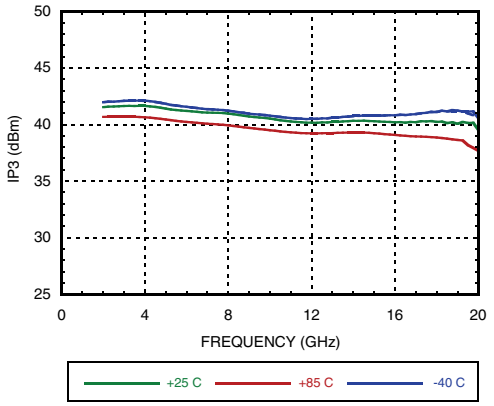
P1dB vs Supply Voltage



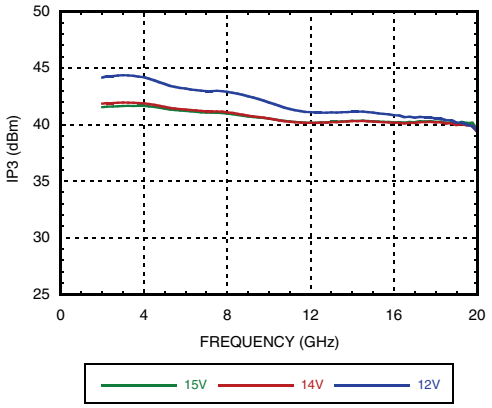
Psat vs. Supply Voltage



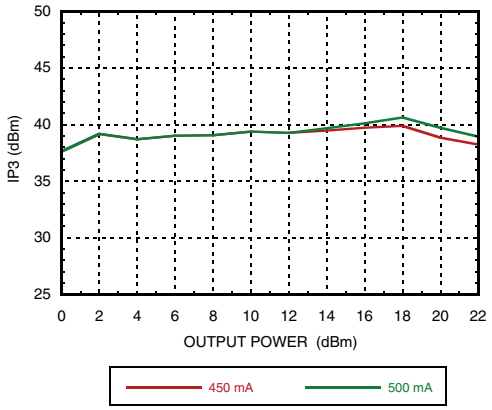
Output IP3 vs. Temperature, Pout/tone = +18 dBm



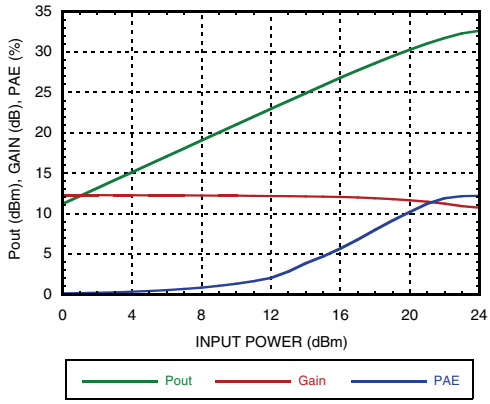
Output IP3 vs. Supply Voltage, Pout/tone = +18 dBm



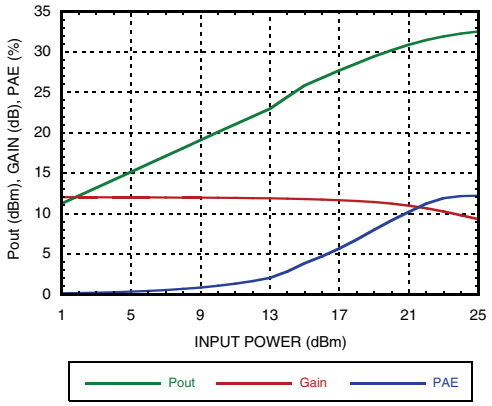
Output IP3 vs. Idd @ 10 GHz



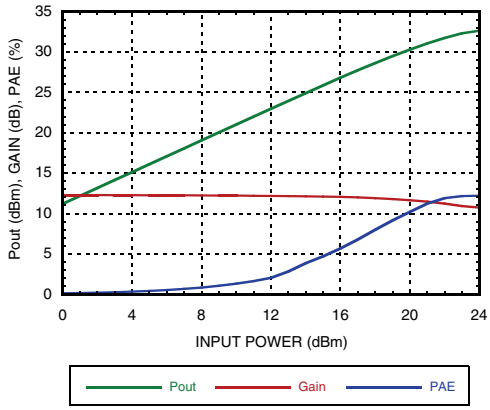
Power Compression @ 4 GHz



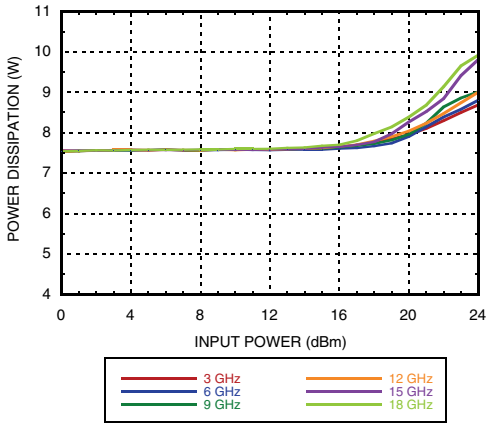
Power Compression @ 10 GHz



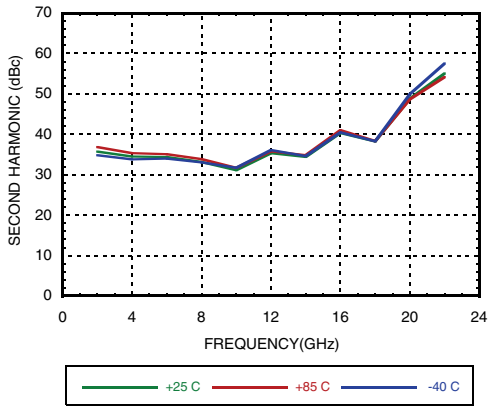
Power Compression @ 18 GHz



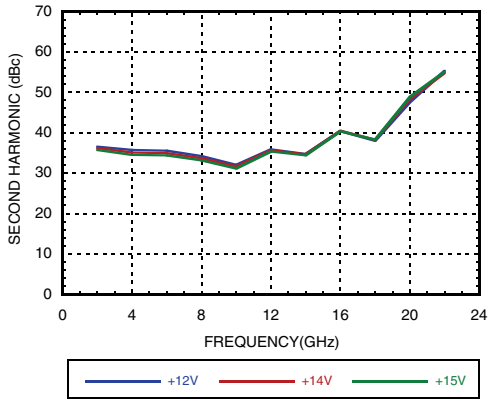
Power Dissipation



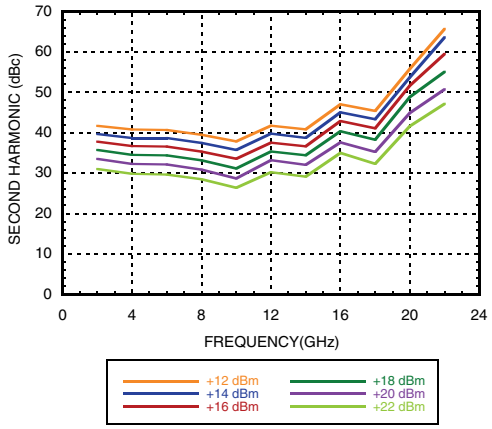
Second Harmonics vs. Temperature @ Pout = 18 dBm



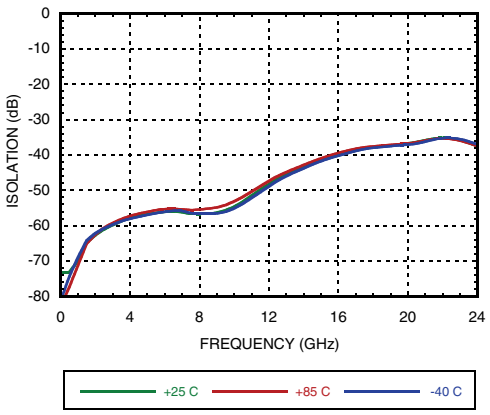
Second Harmonics vs. Vdd @ Pout = 18 dBm



Second Harmonics vs Pout



Reverse Isolation vs. Temperature



Absolute Maximum Ratings

Drain Bias Voltage (Vdd)	+17 Vdc
Gate Bias Voltage (Vgg1)	-3 to 0 Vdc
Gate Bias Voltage (Vgg2)	Vgg2 = (Vdd-6.5V) to (Vdd-4.5V)
RF Input Power (RFIN)	+27 dBm
Channel Temperature	150 °C
Continuous Pdiss (T= 85 °C) (derate 127 mW/°C above 85 °C)	8.26 W
Thermal Resistance (channel to gnd paddle)	7.87 °C/W
Output Power into VSWR > 7:1	+32 dBm
Storage Temperature	-65 to 150°C
Operating Temperature	-40 to 85 °C
ESD Sensitivity (HBM)	Class 1A

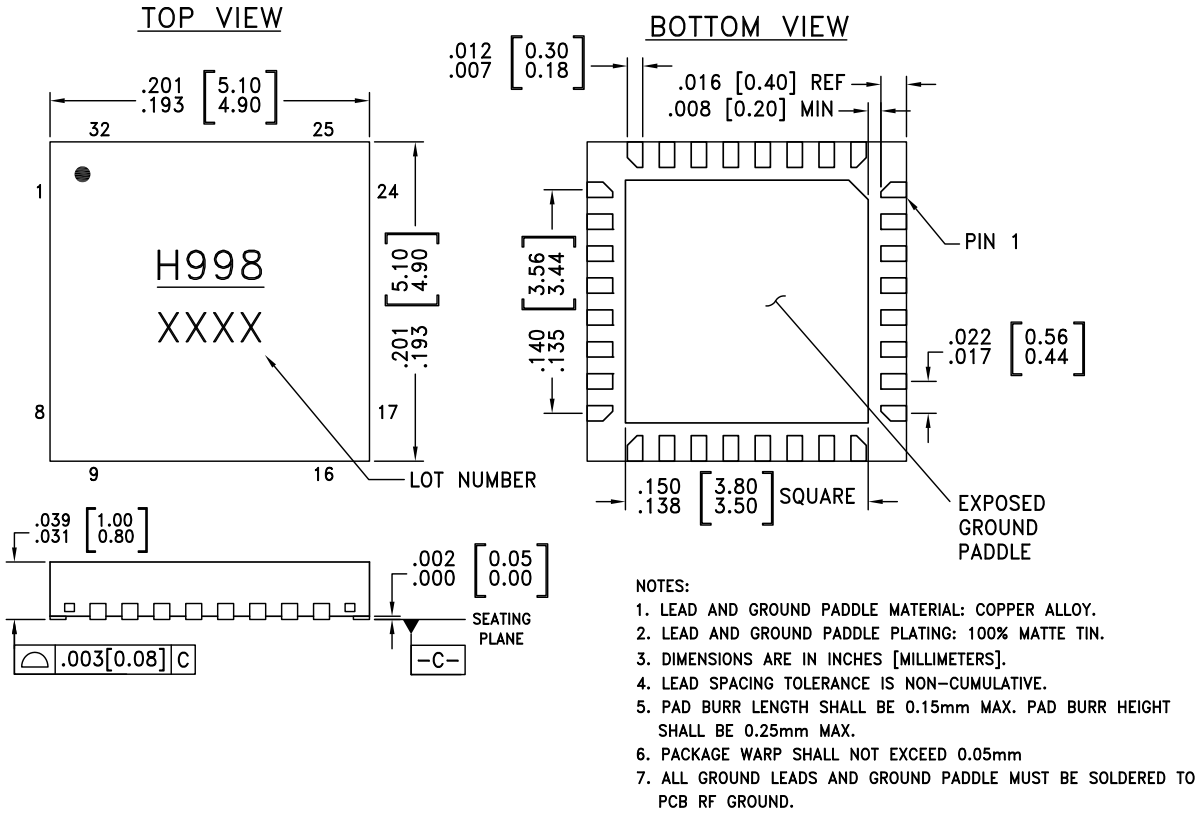
Typical Supply Current vs. Vdd

Vdd (V)	Idd (mA)
+15	500
+14	500
+13	500
+12	500

Adjust Vgg1 to achieve Idd = 500 mA

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



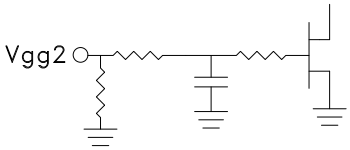
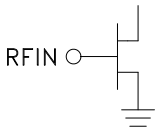
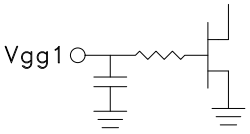
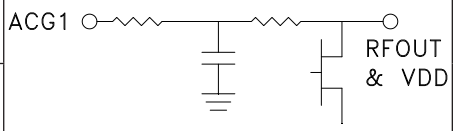
NOTES:
1. LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY.
2. LEAD AND GROUND PADDLE PLATING: 100% MATTE TIN.
3. DIMENSIONS ARE IN INCHES [MILLIMETERS].
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
5. PAD BURR LENGTH SHALL BE 0.15mm MAX. PAD BURR HEIGHT SHALL BE 0.25mm MAX.
6. PACKAGE WARP SHALL NOT EXCEED 0.05mm
7. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.

Package Information

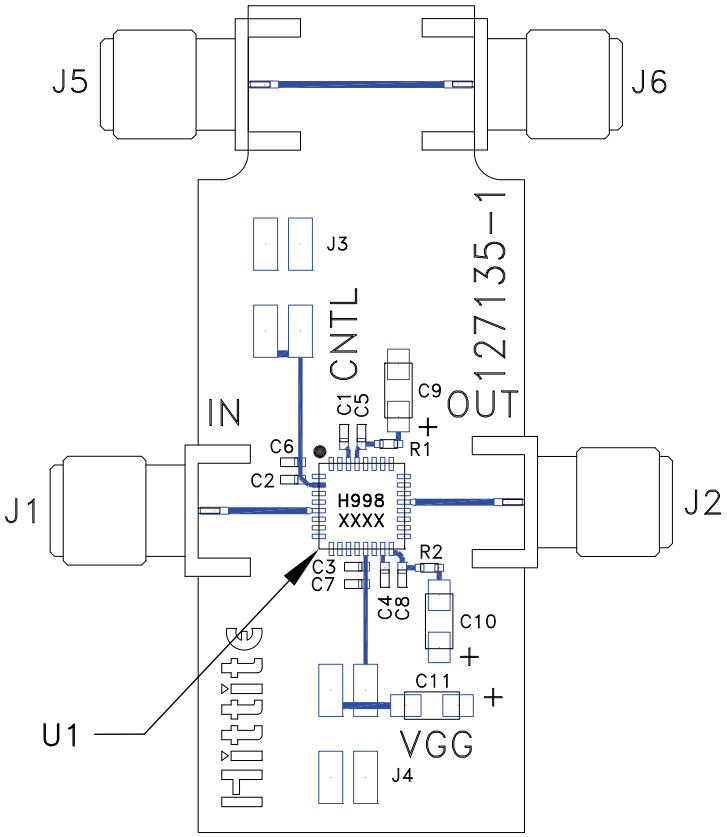
Part Number	Package Body Material	Lead Finish	MSL Rating [2]	Package Marking [1]
HMC998LP5E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL3	H998 XXXX

[1] 4-Digit lot number XXXX
[2] Max peak reflow temperature of 260 °C

Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 4, 6, 14, 20, 22,	GND	These pins and package bottom must be connected to RF/DC ground.	
2	Vgg2	Gate control for amplifier. Attach bypass capacitor per application circuit herein. For nominal opperation +9.5V should be applied to Vgg2.	
3, 7, 8, 9, 10, 11, 12, 17, 18, 19, 23, 24, 25, 26, 27, 28, 31, 32	N/C	These pins are not connected internally, however all data shown herein was measured with these pins connected to RF/DC ground externally.	
5	RFIN	This pad is DC coupled and matched to 50 Ohms. Blocking capacitor is required.	
13	Vgg1	Gate control 1 for amplifier. Attach bypass capacitor per application circuit herein. Please follow “MMIC Biasing Procedure” application note.	
15, 29	ACG4, ACG2	Low frequency termination. Attach bypass capacitor per application circuit.	
21	RFOUT & VDD	RF output for amplifier. Connect DC bias (Vdd) network to provide drain current (Idd). See application circuit herein.	
30	ACG1	Low frequency termination. Attach bypass capacitor per application circuit herein.	

Evaluation PCB



Evaluation Order Information

Item	Contents	Part Number
Evaluation PCB Only	HMC998LP5E Evaluation PCB	Eval01-HMC998LP5E [1]

[1] Reference this number when ordering Evaluation PCB Only

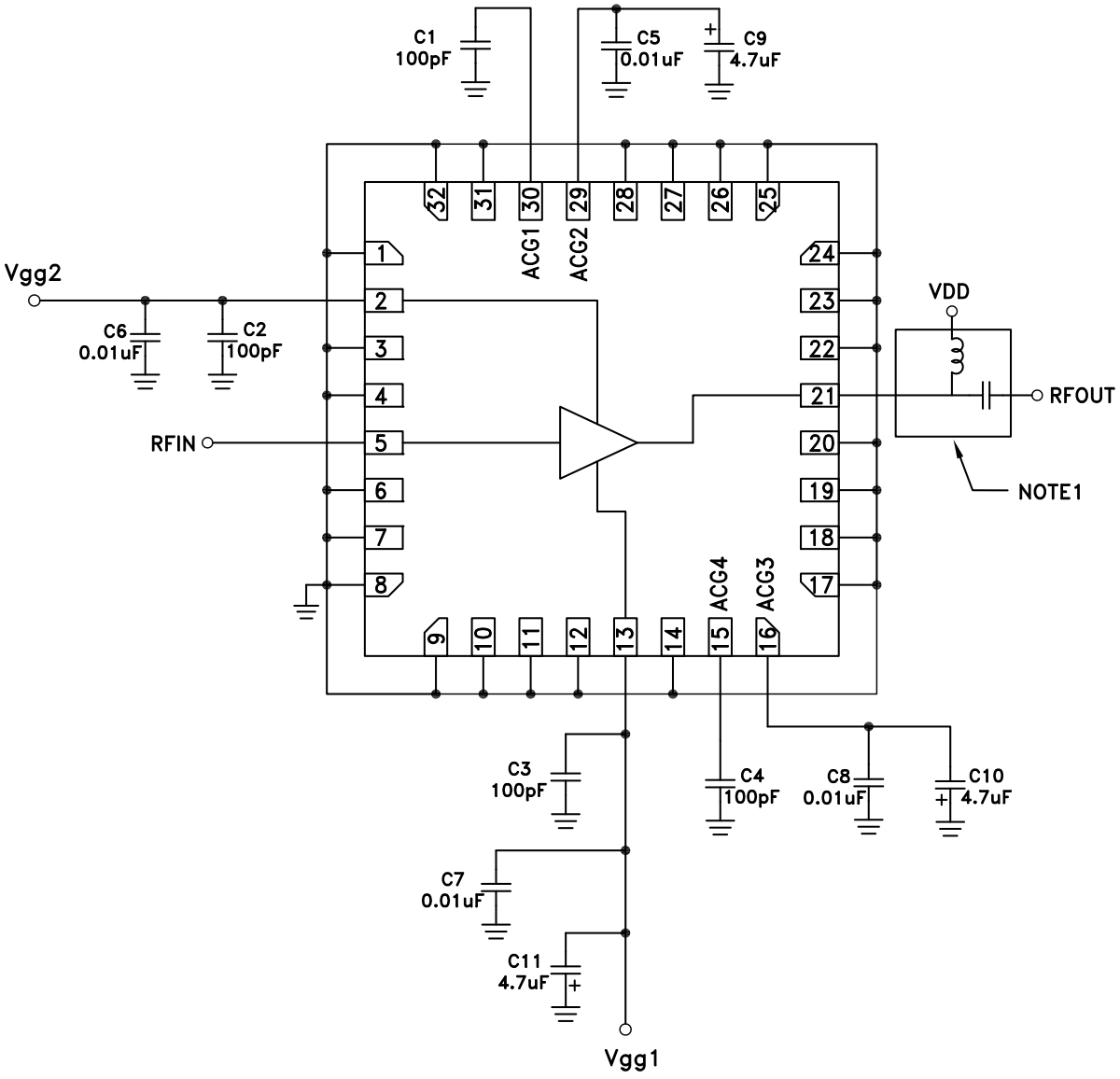
List of Materials for Evaluation PCB EVAL01-HMC998LP5E

Item	Description
J1, J2, J5, J6	PCB Mount SMA RF Connector
J3, J4	DC Pins.
C1 - C4	1000 pF Capacitor, 0402 Pkg.
C5 - C8	10 kpF Capacitor, 0402 Pkg.
C9 - C11	4.7 uF Capacitor, Tantalum.
R1, R2	0 Ohm Resistor, 0402 Pkg.
U1	HMC998LP5E
PCB [1]	127135 Evaluation PCB.

[1] Circuit Board Material: Rogers 4350 or Arlon 25FR

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Application Circuit



NOTE 1: Drain Bias (Vdd) must be applied through a broadband bias tee or external bias network.

Notes: